CH7518 USB-C / DP 1.4 / HDMI 2.0 to 2 ports MIPI Converter

FEATURES

General

- DP and HDMI combo PHY
- DP Receiver compliant with DP specification version 1.4
- DP Receiver supports up to 4 Main Link Lanes at 1.62Gbps,2.7Gbps (HBR), 5.4Gbps (HBR2) and 8.1Gbps (HBR3) link rate
- HDMI Receiver compliant with HDMI specification version 2.0 and DVI specification version 1.0
- HDMI Receiver supports up to 6.0Gbps data rate for video timing of 4Kx2K@60Hz or 1920x1080@240Hz, with TMDS clock frequency up to 594MHz
- HDCP engine compliant with HDCP 2.3 and HDCP 1.4 specification with internal HDCP Keys
- MIPI Transmitter compliant with MIPI D-PHY Specification version 3.0
- MIPI DSI-2 specification version 2.0, and MIPI CSI-2 specification version 4.0
- Bandgap Resistor free
- On-chip Audio encoder which support IIS/ S/PDIF audio output
- Integrated Ra, Rd and Rp resistors for DFP/UFP to identify connection
- Seamless switch between Type-C SBU and DisplayPort AUX Channel
- USB Power Delivery 3.1 on CC communication
- Built-in USB Billboard Class 1.2.2 and USB 2.0 PHY to support DisplayPort Alt-mode
- Progressive 3D video formats supported, with formats of Side-by-Side
- Support DSC pass-through
- MCU embedded to handle the control logic
- Support device boot up by automatically loading firmware from embedded Boot ROM
- IIC slave interface and DP AUX interface are available for configure, debug and firmware update
- Support Auto Power Saving mode and low stand-by current
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 64-pin QFN package (7.5 x 7.5 mm)

USB-C / DP Rx

- USB Type-C port compliant with USB Type-C Cable and Connector Specification revision 2.0
- USB PD 3.1 compliant
- Compliant with DisplayPort Alternate Mode on USB Type C standard
- Compliant with VESA DisplayPort Specification version 1.4 and and Embedded DisplayPort (eDP) Specification version 1.4

GENERAL DESCRIPTION

Chrontel's CH7518 is a low-cost, low-power semiconductor device that consists of a USB-C/DP /HDMI Combo receiver, MIPI DSI/CSI-2 transmitter and audio encoder, which can convert USB-C/DP/HDMI signals with UHD resolution into MIPI outputs at a maximum conversion rate of 594 MHz with resolution up to 4Kx2K@60Hz or 1920x1080@240Hz, and with IIS or SPDIF audio output.

The CH7518's DP receiver is compliant with the DisplayPort Specification 1.4 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7518 supports USB Type-C cable plug orientation switch. The CH7115's HDMI Receiver integrated is compliant with HDMI 2.0. With internal HDCP key Integrated, the device supports HDCP 1.4 and 2.3 specifications. The 2 MIPI output ports meet MIPI D-PHY Specification version 3.0, MIPI DSI specification version 2.0, and MIPI CSI-2 specification version 4.0.

With sophisticated MCU and the on-chip Boot ROM, CH7518 supports auto-boot and EDID buffer. Leveraging the firmware auto loaded from the embedded Boot ROM, CH7518 can support DP input detection and determine to enter into power saving mode automatically.

- Supports up to 4 Main Link Lanes at 1.62Gbps,2.7Gbps (HBR), 5.4Gbps (HBR2) and 8.1Gbps (HBR3) link rate
- Automotive DP input signal detection and Lane swap supported for compliance with the USB type C cable plug orientation switch
- RGB at 6/8/10/12 bpc, YCbCr4:4:4 and YCbCr4:2:2 /4:2:0 at 8/10/12 bpc input formats supported
- Fast and full Link Training for embedded DisplayPort system
- Supports eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- Progressive 3D video formats supported
- Forward Error Correction supported
- Supports Spread Spectrum Clocking (de-spreading) for EMI reduction
- Programmable/Adaptive equalizer to compensate for Cable, PCB and/or connector losses

HDMI Rx

- HDMI Receiver compliant with HDMI specification version 2.0 and DVI specification version 1.0
- HDMI Receiver supports up to 6.0Gbps data rate for video timing of 4Kx2K@60Hz or 1920x1080@240Hz, with TMDS clock frequency up to 594MHz
- Adaptive HDMI Receiver equalization supported for the compensation of input signal attenuation
- Progressive 3D video formats supported
- SCDC supported on HDMI DDC
- TMDS descrambling supported for EMI/RFI reduction
- Integrated EDID Buffer
- HDMI input detection supported
- Audio Return Path, HDMI Ethernet Channels and CEC function NOT supported

MIPI Tx

- MIPI Transmitter compliant with MIPI D-PHY Specification version 3.0
- MIPI DSI-2 specification version 2.0, and MIPI CSI-2 specification version 4.0
- Single/Dual Channel MIPI D-PHY DSI/CSI-2 Tx configurable, with 1/2/3/4 data lanes scalability for each channel, and up to 2.5 Gbps / data lane supported to transmit video with timing up to 4Kx2K@60Hz or 1920x1080@240Hz within 8 data lane configuration
- Deskew calibration sequence initialization support
- Programmable transmitter swing and pre-emphasis
- Lane swap and polarity inversion supported
- Left / Right frames mode or odd /even alternative pixels mode 3D video formats output support
- DSI Burst mode and non-burst mode output support
- Video data formats RGB565, RGB666, RGB888, YCbCr444, YCbCr 422 and YCbCr 420 supported with deep color depth up to 12 bits
- Programmable Panel Power Sequence Control support

APPLICATION

- Pro-AV Devices
- Handheld/Portable Devices
- Car Infotainment Devices
- Industrial Devices

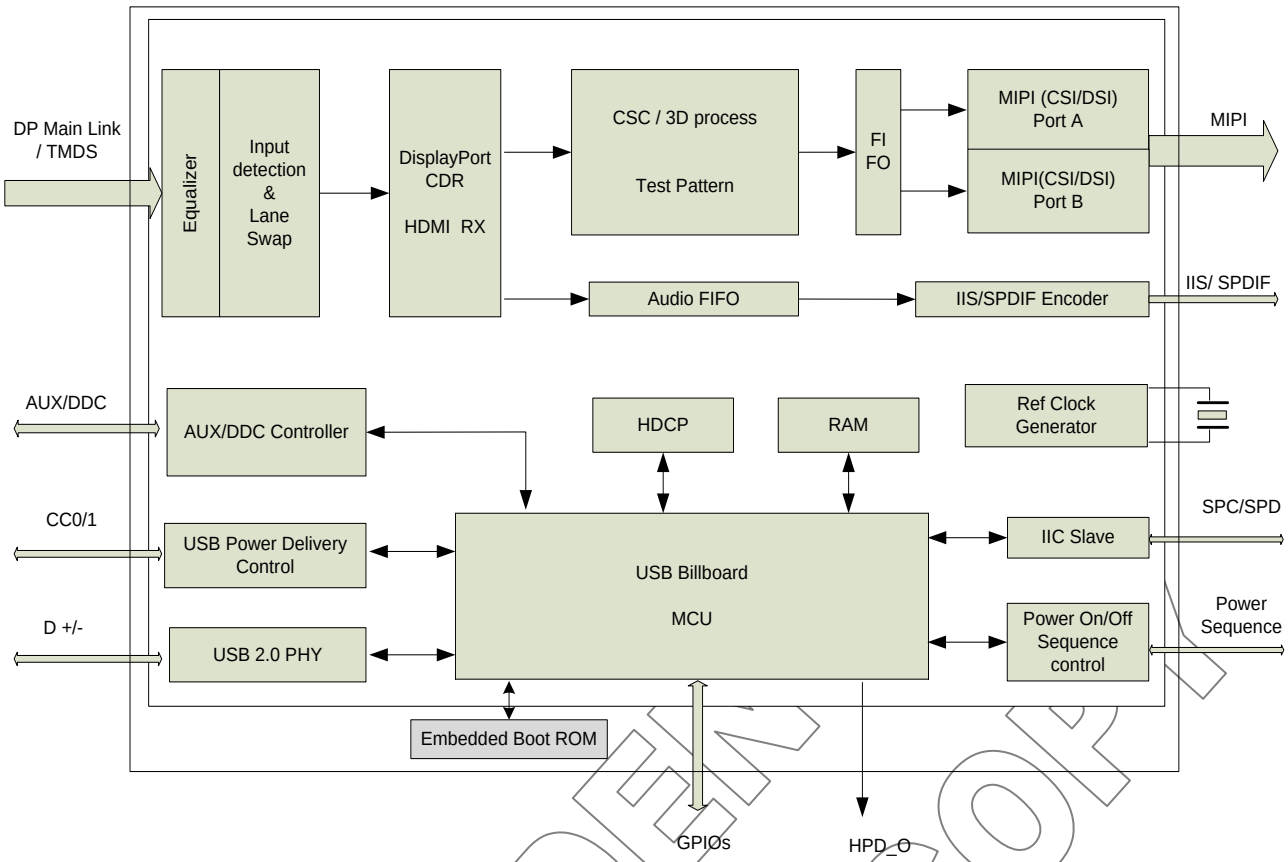

Figure 1: CH7518 Functional Block Diagram

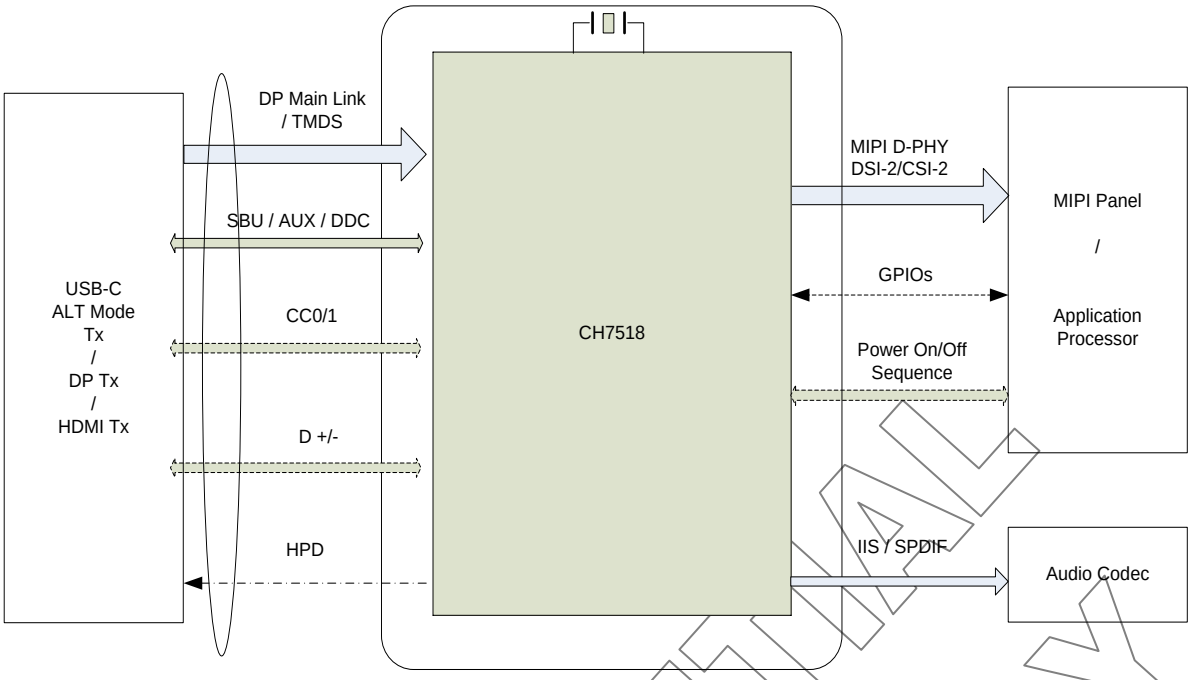

Figure 2: CH7518 Application Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

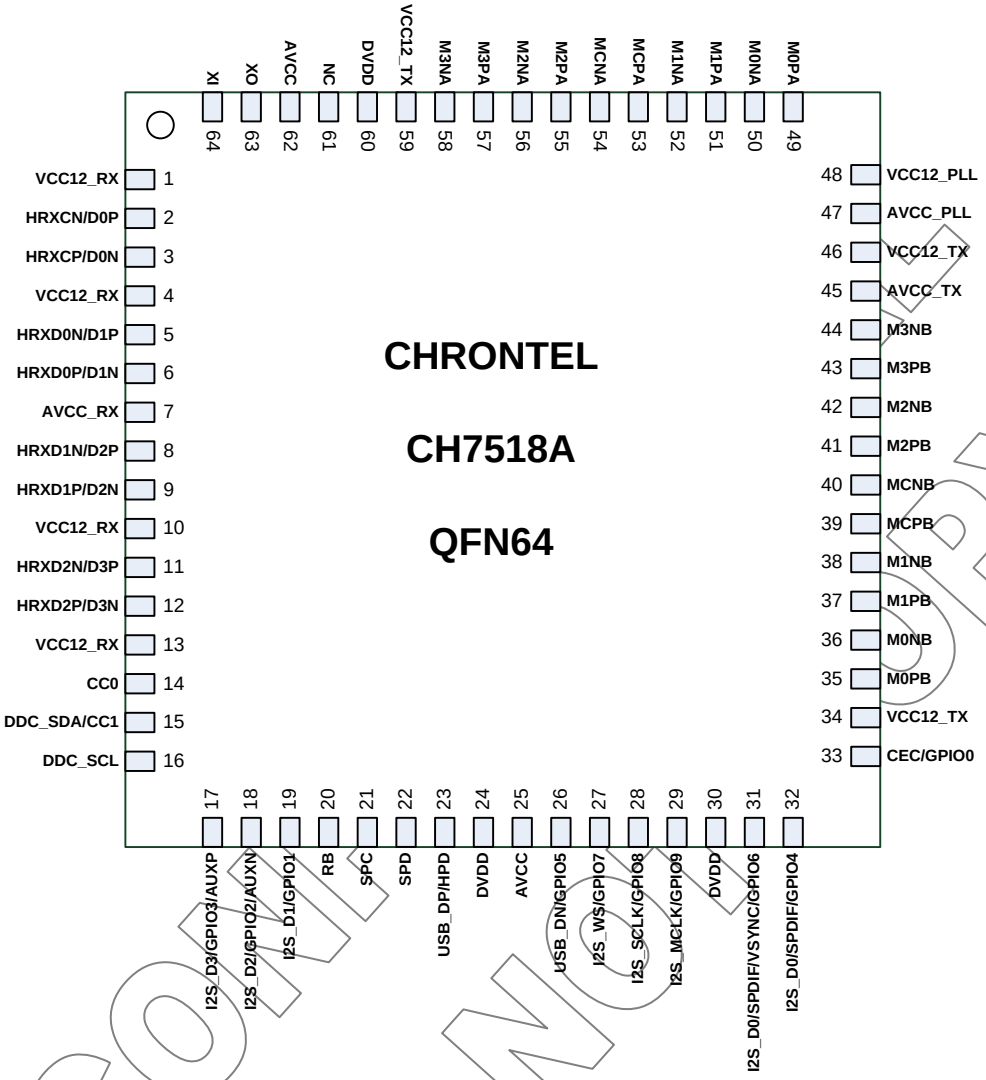

Figure 3: CH7518 64 pin QFN Package

1.2 Pin Description

Table 1: CH7518 Pin Name Descriptions

Pin #	Type	Symbol	Description
2,3,5,6,8,9, 11,12	In	HRXCP/N, HRXD[2:0]P/N, D[3:0]P/N	**HDMI TMDS / DP Main Link Differential Input** These pins accept four DC or AC-coupled differential pair signals from the HDMI/DisplayPort transmitter.
14	In/Out	CC0	**USB Type-C Configure Channel 0**
15	In/Out	CC1	**USB Type-C Configure Channel 1**
	In/out	DDC_SDA	**Serial Port Data to HDMI/DVI Transmitter** This pin functions as the data bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level
16	In	DDC_SCL	**Serial Port Clock to HDMI/DVI Transmitter** This pin functions as the clock bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level
17	In/Out	AUXP	**AUX Channel Positive Input/Output** This pin is DisplayPort AUX Channel positive pin
	Out	I2S_D3/SPDIF	**I2S Serial Data 3 or SPDIF Output**
	In/out	GPIO3	**General Purpose Input/Output**
18	In/Out	AUXN	**AUX Channel Negative Input/Output** This pin is DisplayPort AUX Channel negative pin
	Out	I2S_D2	**I2S Serial Data 2**
	In/out	GPIO2	**General Purpose Input/Output**
19	In/Out	GPIO1	**General Purpose Input/Output**
	Out	I2S_D1	**I2S Serial Data 1**
20	In	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
21	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
22	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required
23	Out	HPD	**DisplayPort Receiver Hot Plug output**
	In/Out	USB_DP	**D+ Input of USB Type C Interface**
26	In/Out	USB_DN	**D- Input of USB Type C Interface**
	In/Out	GPIO5	**General Purpose Input/Output**
27	In/Out	GPIO7	**General Purpose Input/Output**
	Out	I2S_WS	**I2S Word Select**
28	Out	I2S_SCLK	**I2S Continuous Serial Clock**
	In/Out	GPIO8	**General Purpose Input/Output**
29	Out	I2S_MCLK	**I2S System Clock**
	In/Out	GPIO9	**General Purpose Input/Output**
31	Out	I2S_D0	**I2S Serial Data 0 Output**

	Out	SPDIF	**SPDIF Output**
	Out	VSYNC	**Vsync Output**
	In/Out	GPIO6	**General Purpose Input/Output**
32	Out	I2S_D0	**I2S Serial Data 0 Output**
	Out	SPDIF	**SPDIF Output**
	In/Out	GPIO4	**General Purpose Input/Output**
33	In/out	CEC	**HDMI CEC Pin**
	In/Out	GPIO0	**General Purpose Input/Output**
35~44	Out	M[3:0]P/NB MCP/NB	**MIPI TX Port B**
49~58	Out	M[3:0]P/NA MCP/NA	**MIPI TX Port A**
61	NC	NC	**Not Connected**
63	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
64	In	XI	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock also can drive the XI Input
1,4,10,13,34,46,48,59	Power	VCC12_RX VCC12_TX	**DisplayPort Receiver/MIPI Transmitter Analog Power Supply (1.2V)**
7, 25, 45,47,62	Power	AVCC_RX AVCC_TX AVCC	**Analog Power Supply (3.3V)**
24,30,60	Power	DVDD	**Digital Core Power Supply (1.2V)**
Pad	Power	GND	**Power Supply Ground**

2.0 PACKAGE DIMENSION

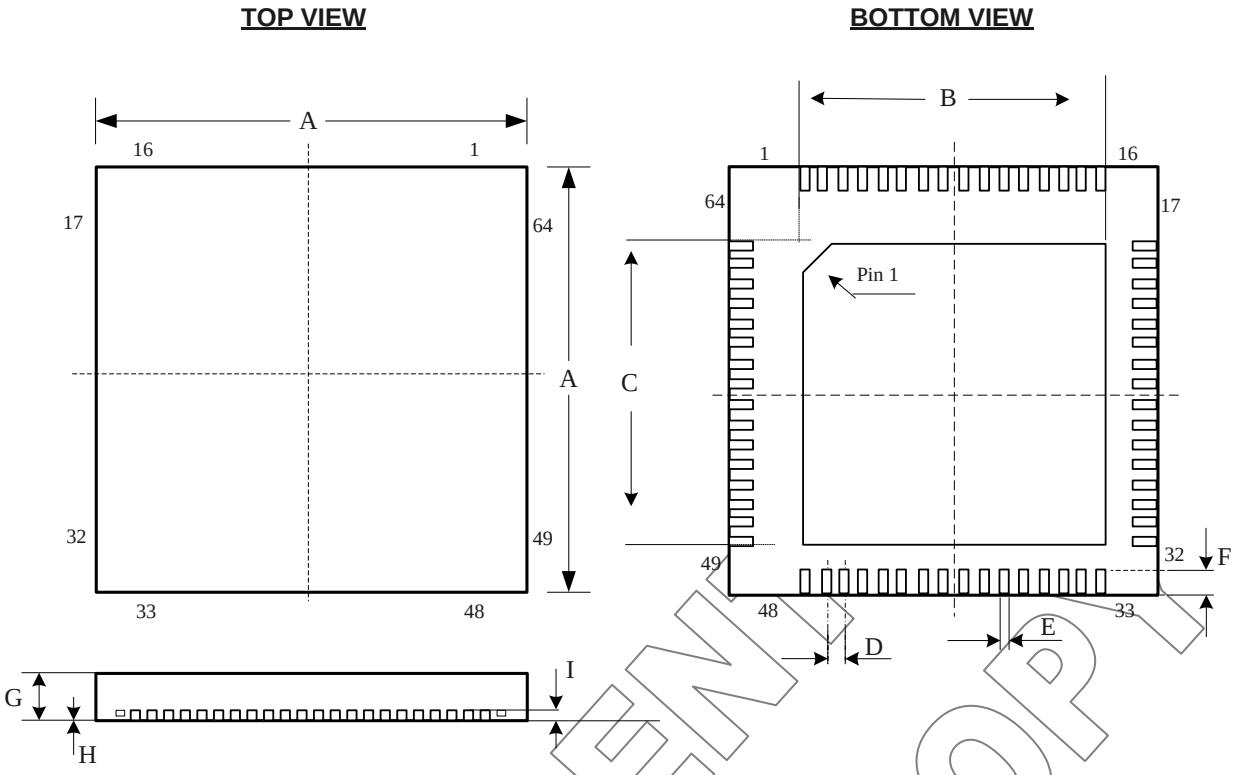

Figure 4: 64 Pin QFN Package (7.5x7.5 mm)

Table of Dimensions

No. of Leads		SYMBOL								
64 (7.5x7.5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.40	6.10	6.10	0.40 BSC	0.15	0.35	0.70	0.00	0.203 REF
	MAX	7.60	6.30	6.30		0.25	0.45	0.80	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.
2. All dimensions DO NOT include MOLD FLASH or PROTRUSION.

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ORDERING INFORMATION

Part Number	Package Type	Content Protection	Operating Temperature Range	Minimum Order Quantity
CH7518A-BF	64 QFN, Lead-free	None	Commercial : 0 to 70°C	**260/Tray**
CH7518A -BFK	64 QFN, Lead-free	HDCP 2.3 / 1.4	Commercial : 0 to 70°C	**260/Tray**
CH7518A -BFI	64 QFN, Lead-free	None	Industrial : -40 to 85°C	**260/Tray**
CH7518A -BFIK	64 QFN, Lead-free	HDCP 2.3 / 1.4	Industrial : -40 to 85°C	**260/Tray**

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